

*Fig. 1*

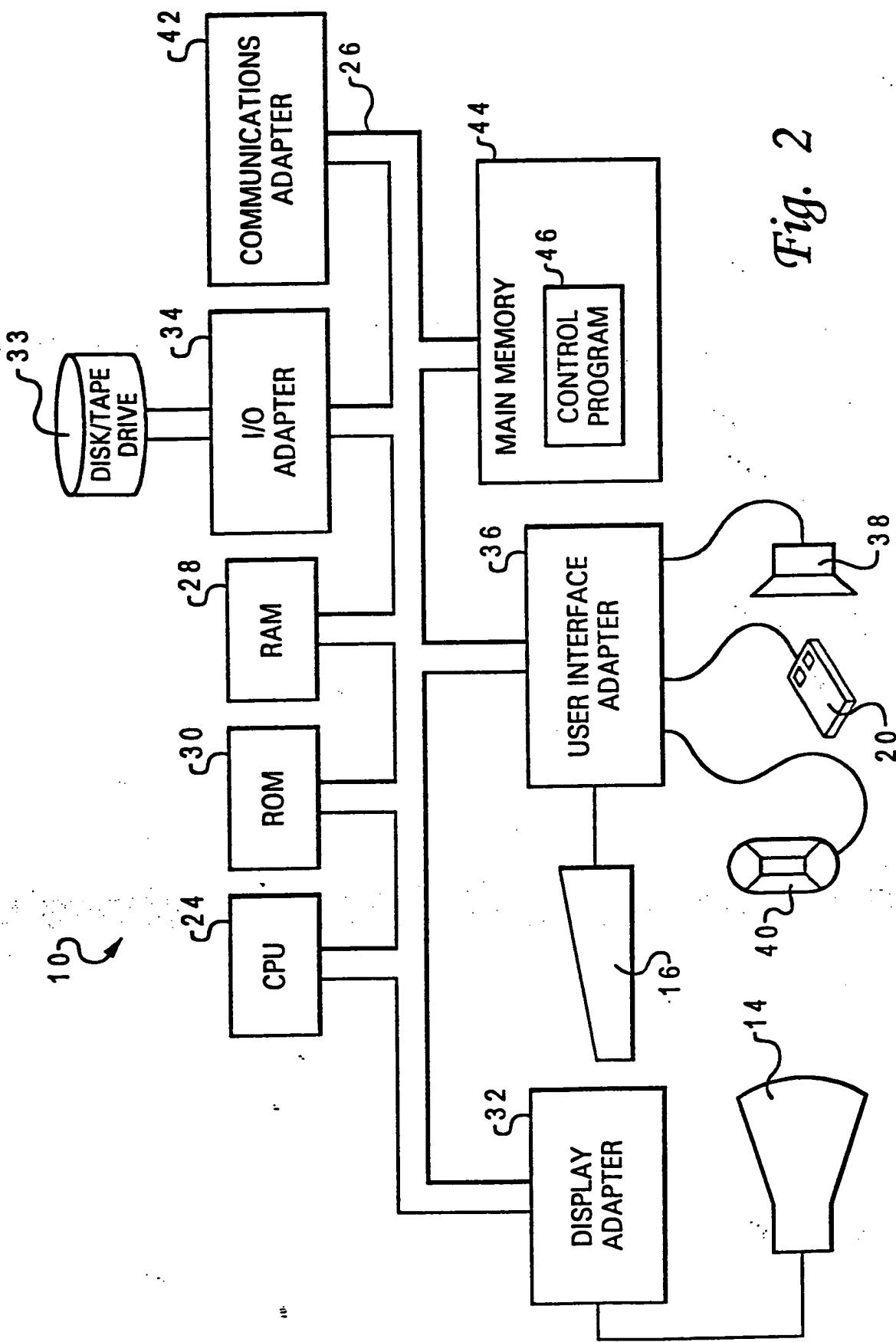


Fig. 2

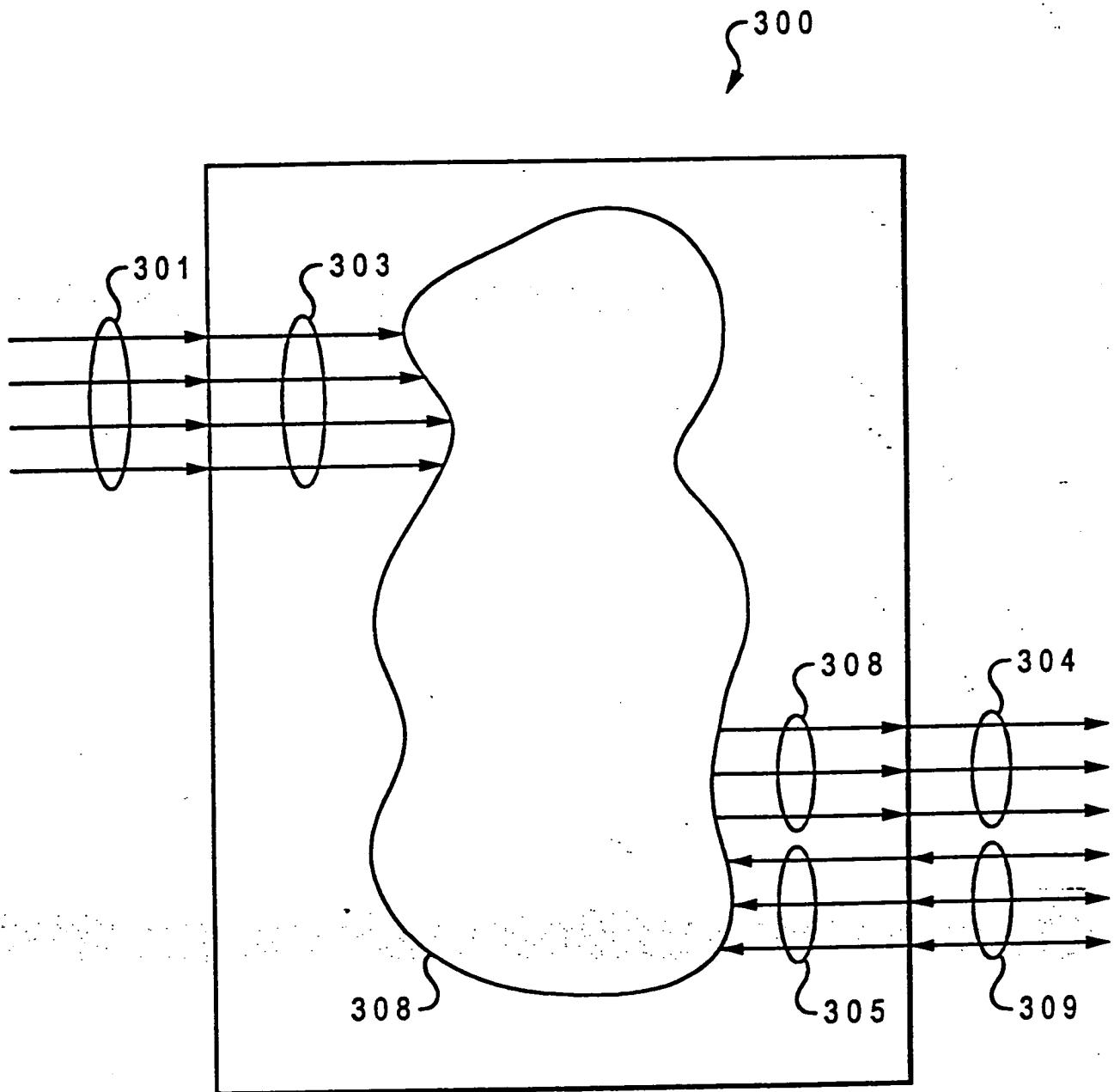


Fig. 3A

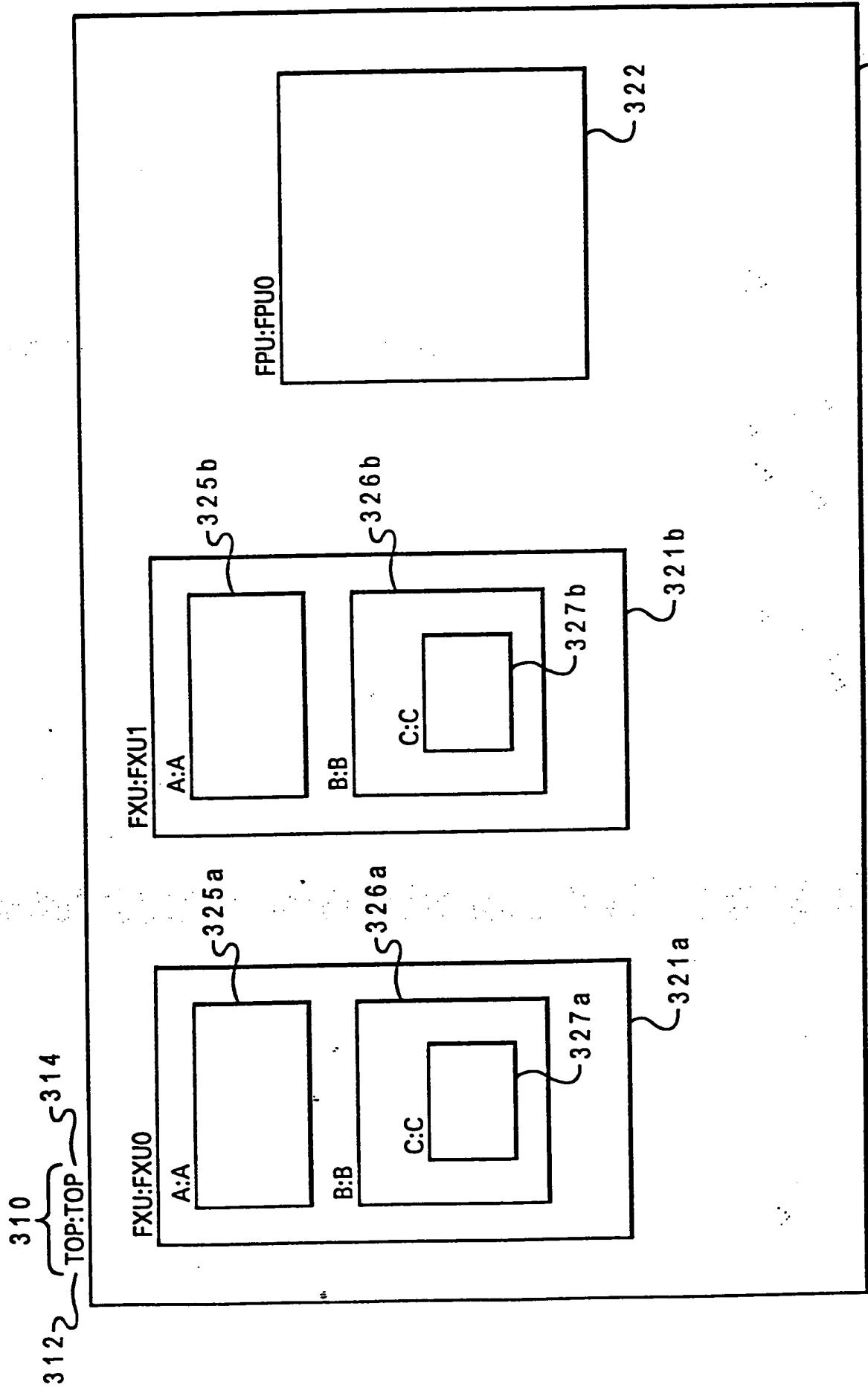


Fig. 3B

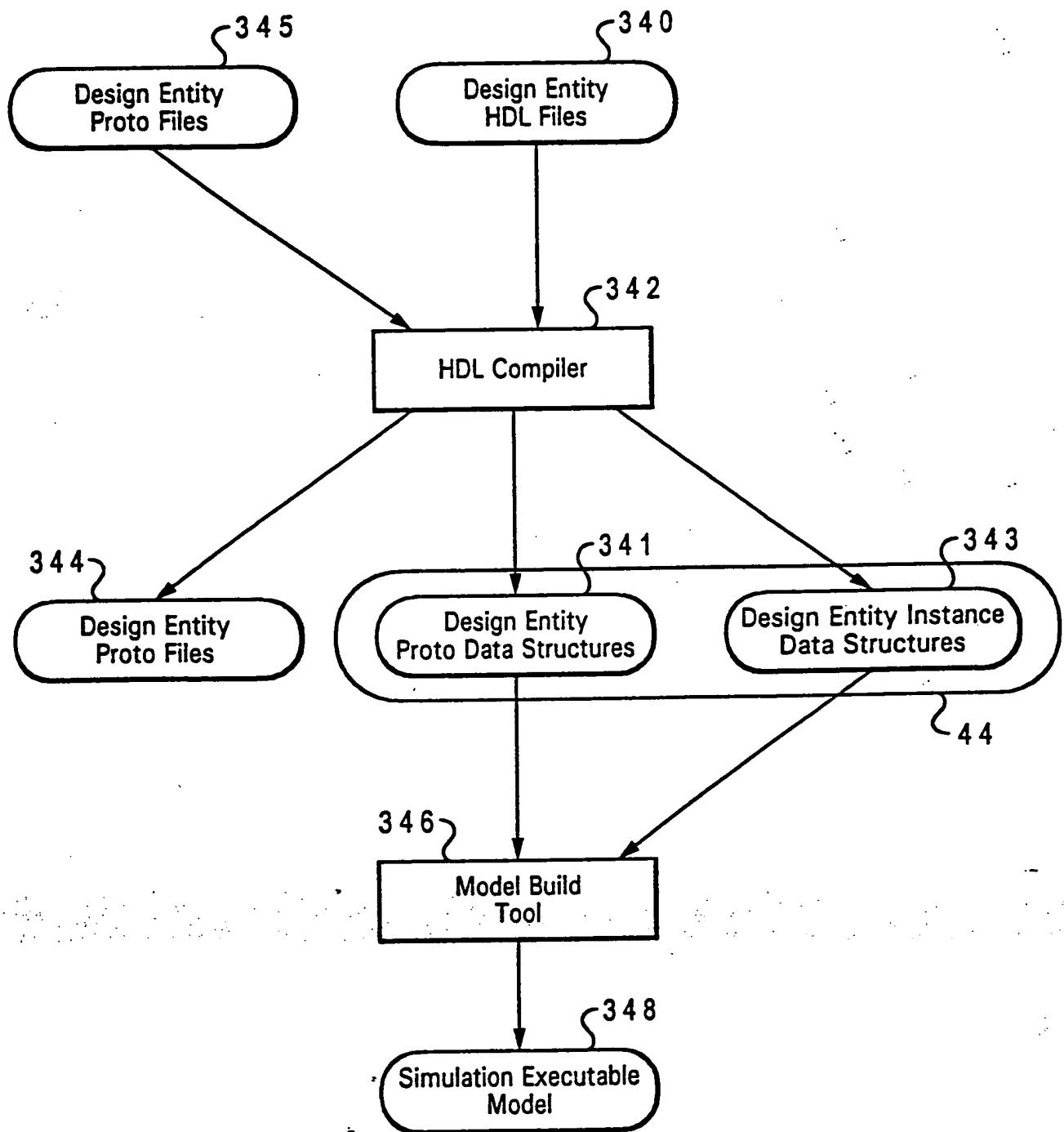


Fig. 3C

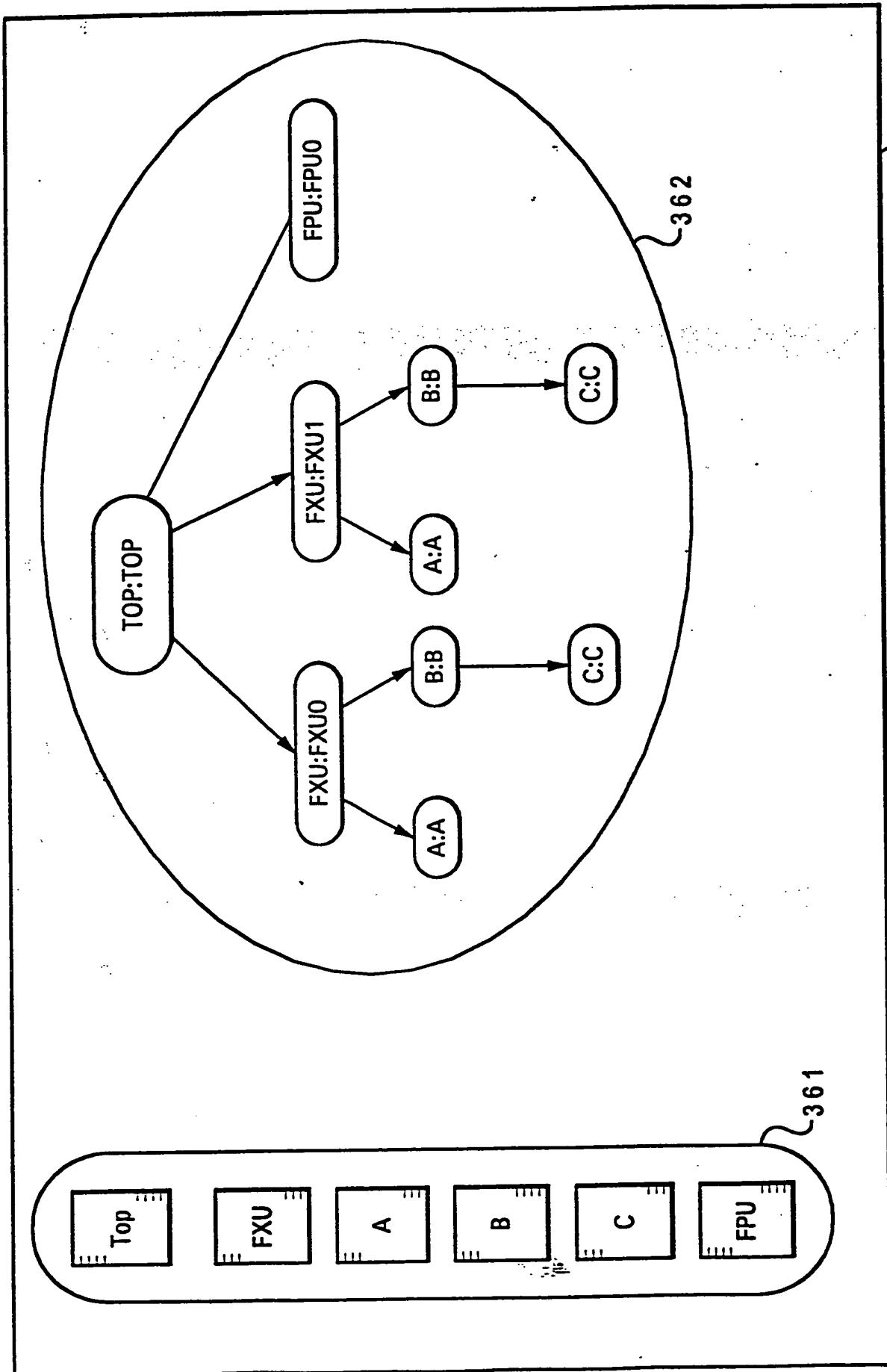


Fig. 3D

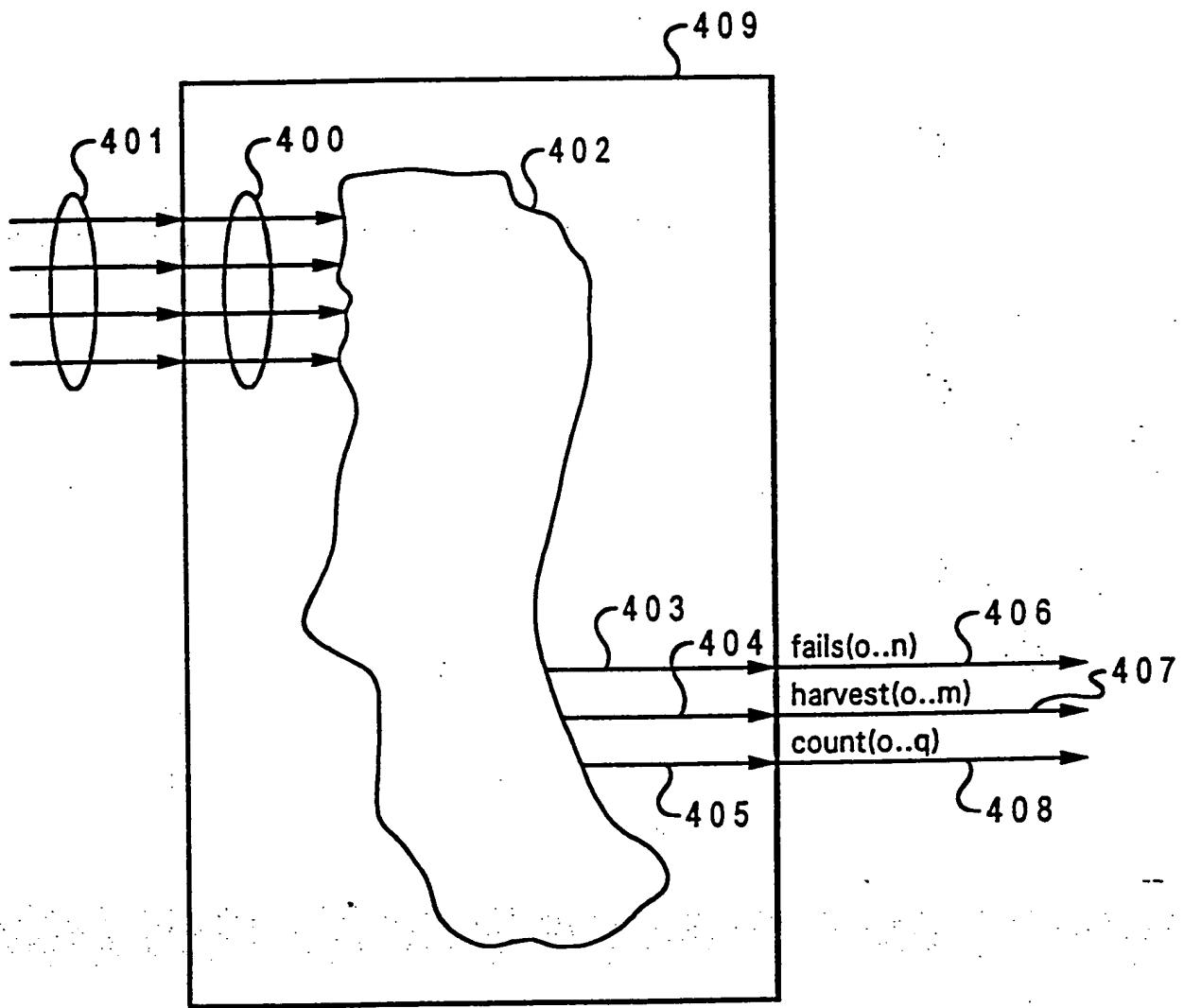


Fig. 4A

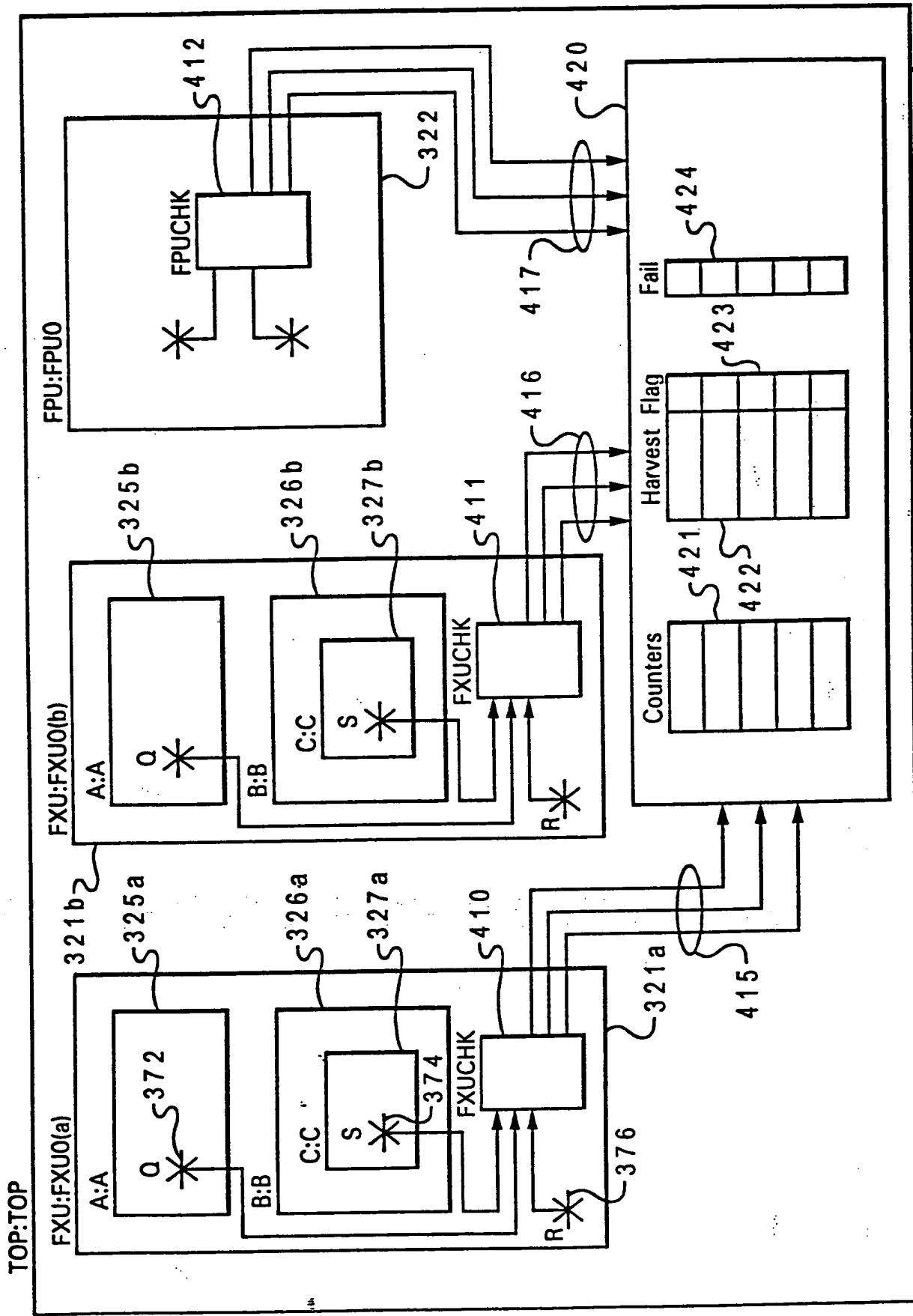


Fig. 4B

ENTITY FXUCHK IS

```
PORT( S_IN      : IN std_ulogic;
       Q_IN      : IN std_ulogic;
       R_IN      : IN std_ulogic;
       clock     : IN std_ulogic;
       fails     : OUT std_ulogic_vector(0 to 1);
       counts    : OUT std_ulogic_vector(0 to 2);
       harvests  : OUT std_ulogic_vector(0 to 1);
);
```

450

452 {  
-!! BEGIN  
-!! Design Entity: FXU;

453 {  
-!! Inputs  
-!! S\_IN => B.C.S;  
-!! Q\_IN => A.Q;  
-!! R\_IN => R;  
-!! CLOCK => clock;  
-!! End Inputs

454 {  
-!! Fail Outputs;  
-!! 0 : "Fail message for failure event 0";  
-!! 1 : "Fail message for failure event 1";  
-!! End Fail Outputs;

455 {  
-!! Count Outputs;  
-!! 0 : <event0> clock;  
-!! 1 : <event1> clock;  
-!! 2 : <event2> clock;  
-!! End Count Outputs;

456 {  
-!! Harvest Outputs;  
-!! 0 : "Message for harvest event 0";  
-!! 1 : "Message for harvest event 1";  
-!! End Harvest Outputs;

457 {  
-!! End;

440

451

ARCHITECTURE example of FXUCHK IS

BEGIN

... HDL code for entity body section ...

END;

458

Fig. 4C

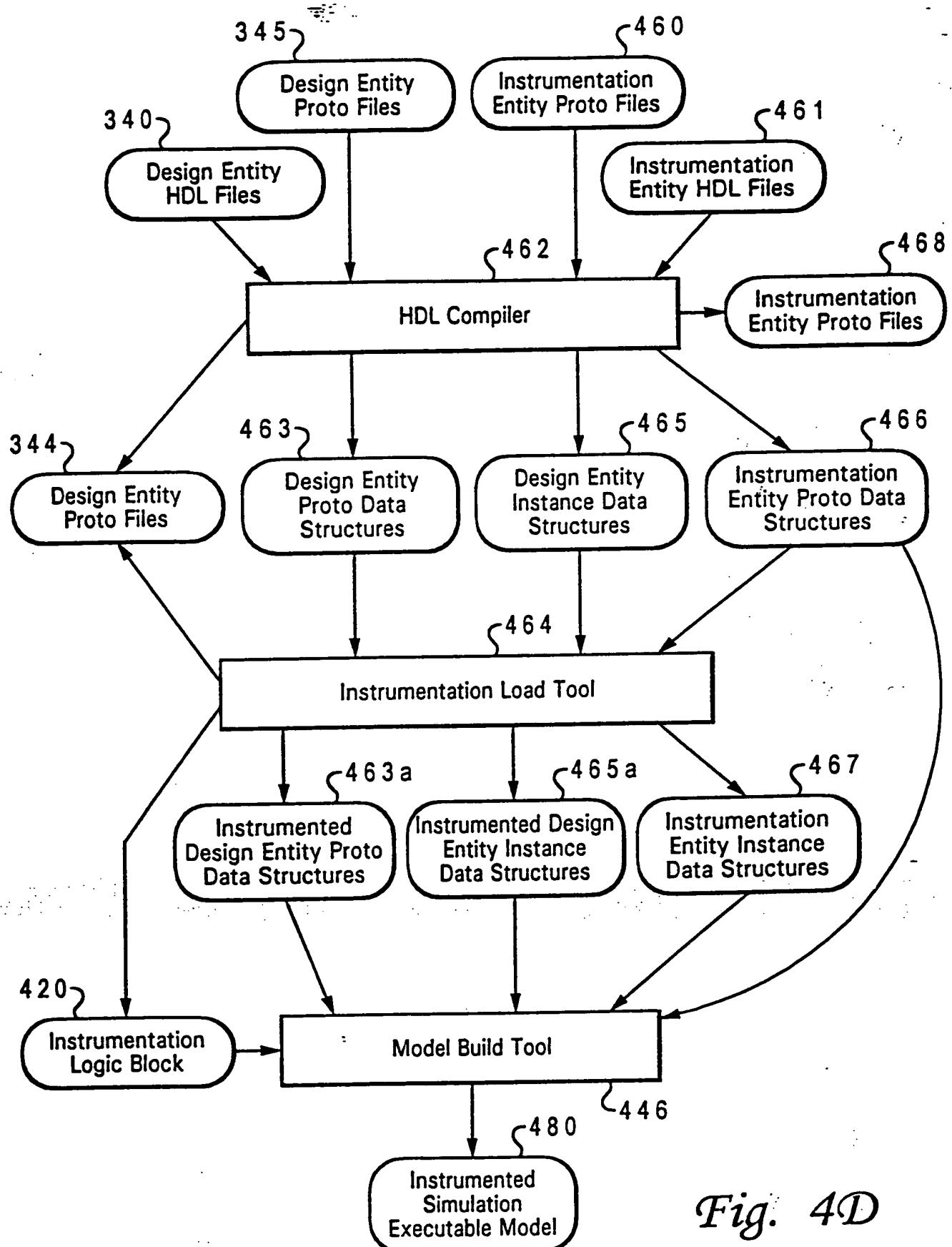


Fig. 4D

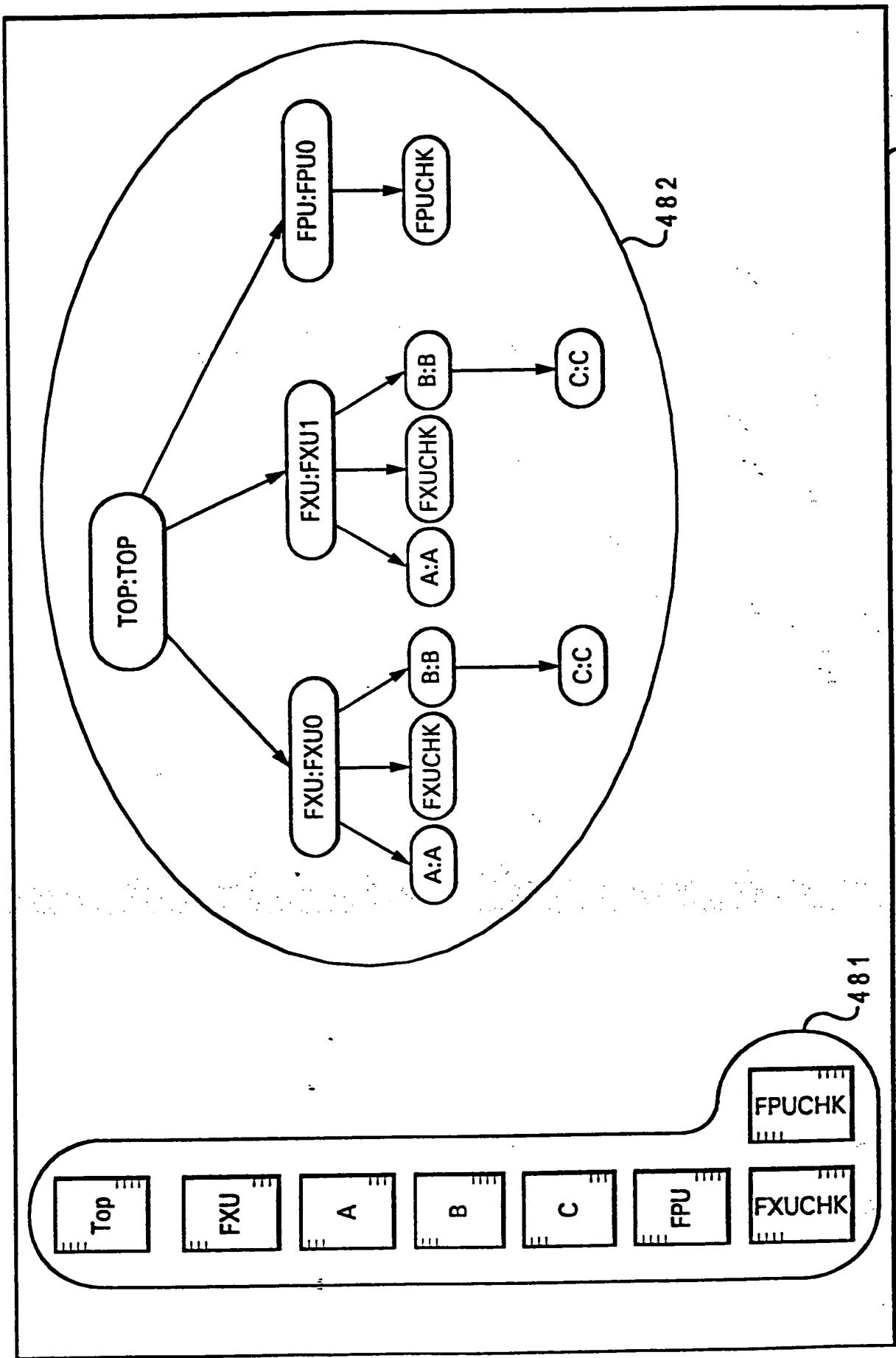


Fig. 4E

44

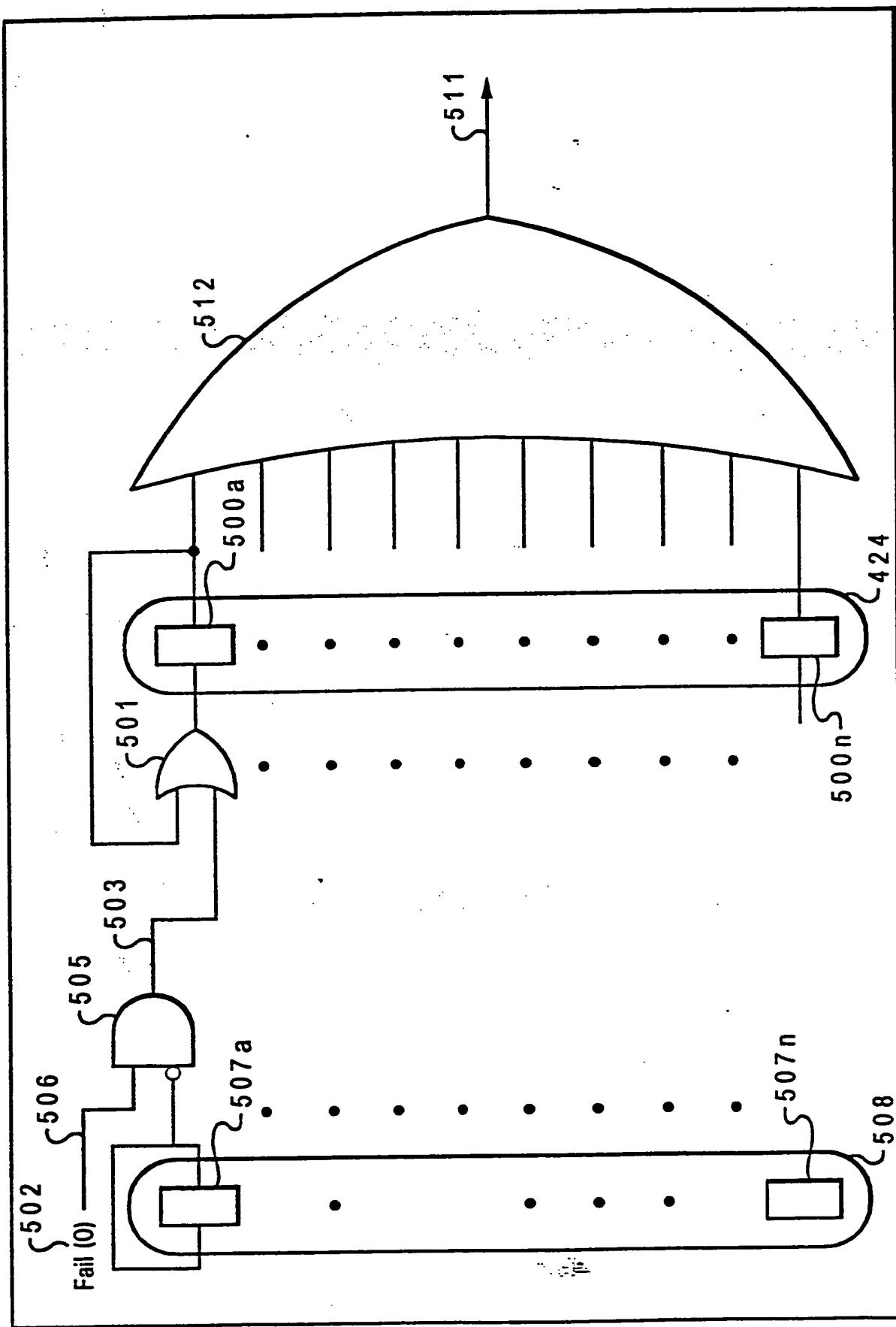


Fig. 5A

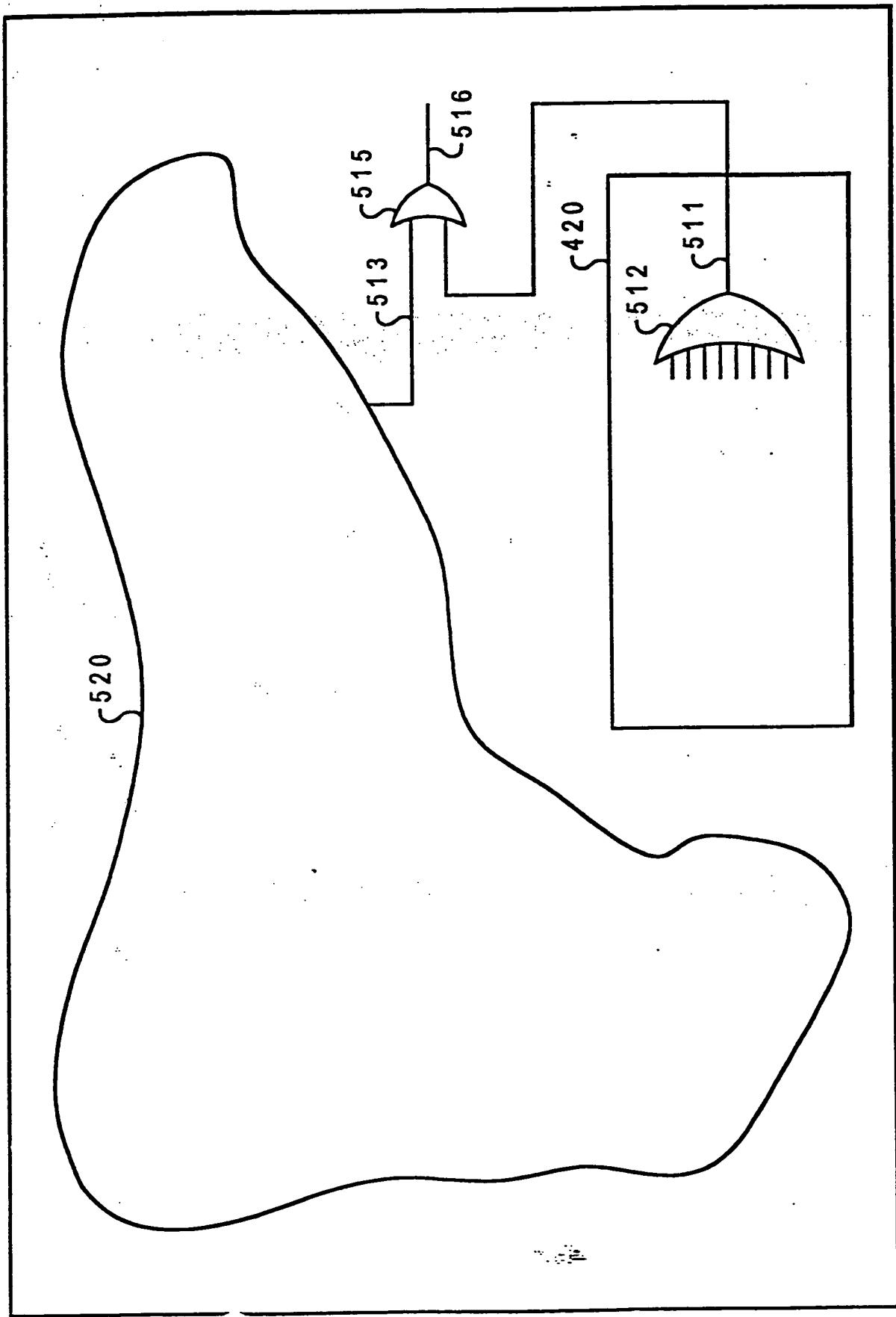


Fig. 5B

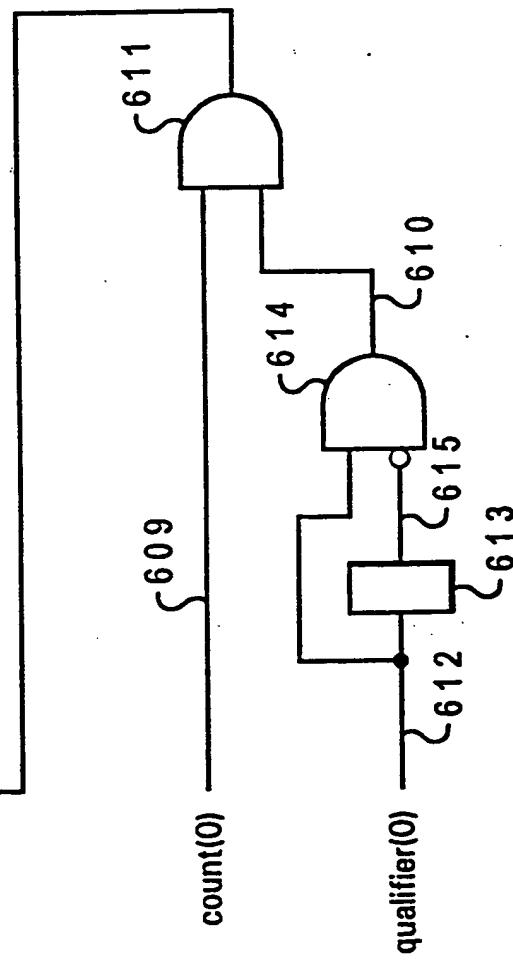
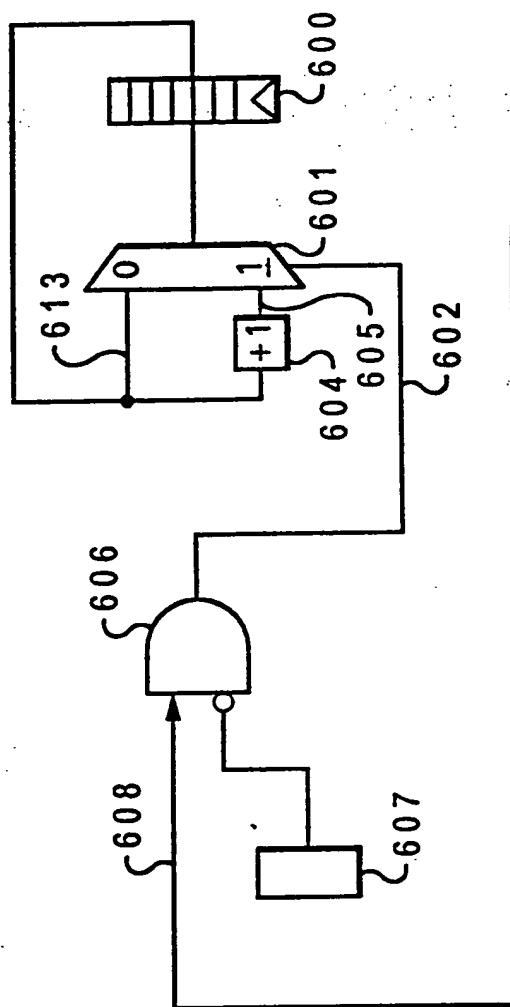
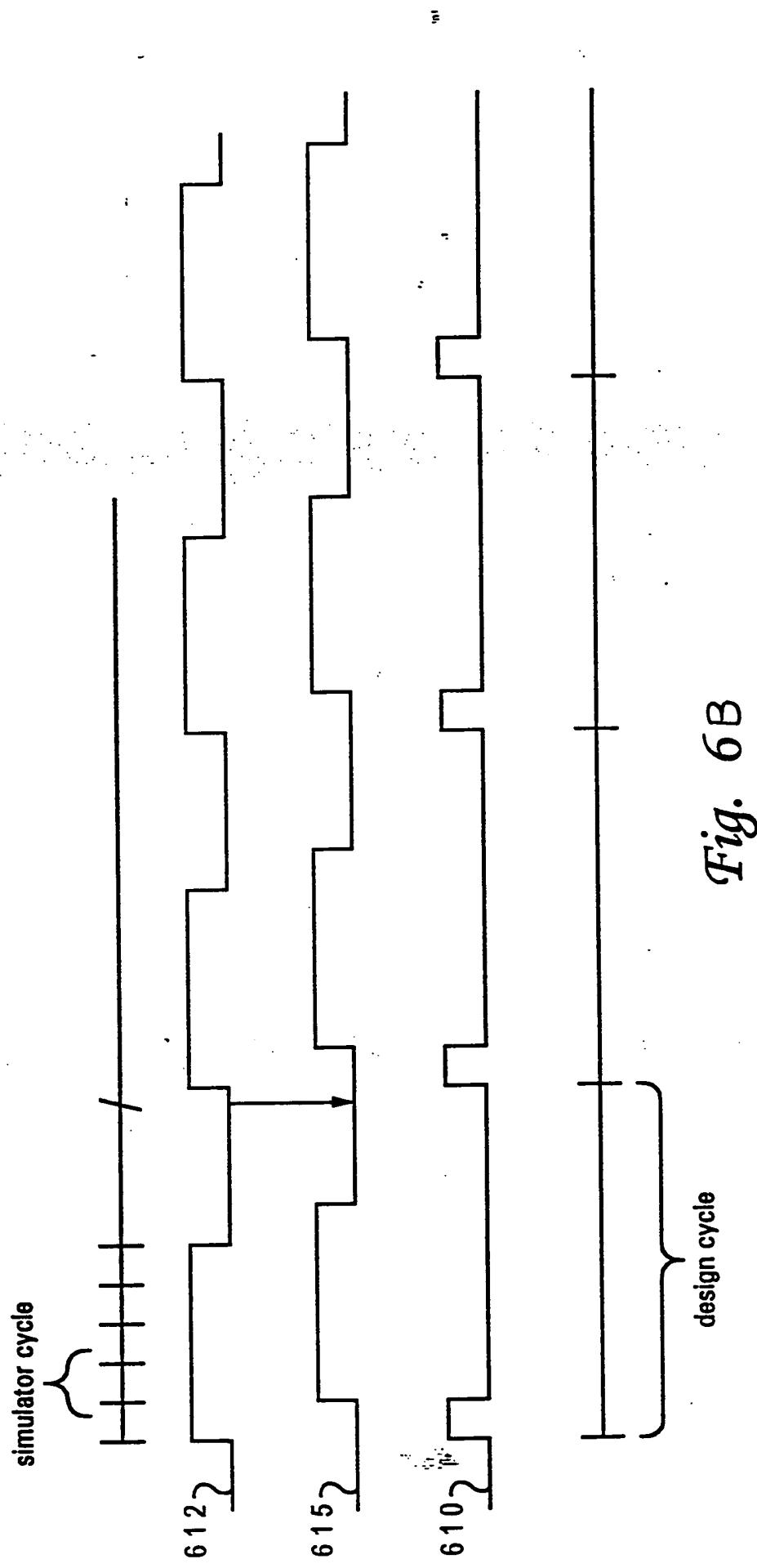


Fig. 6A

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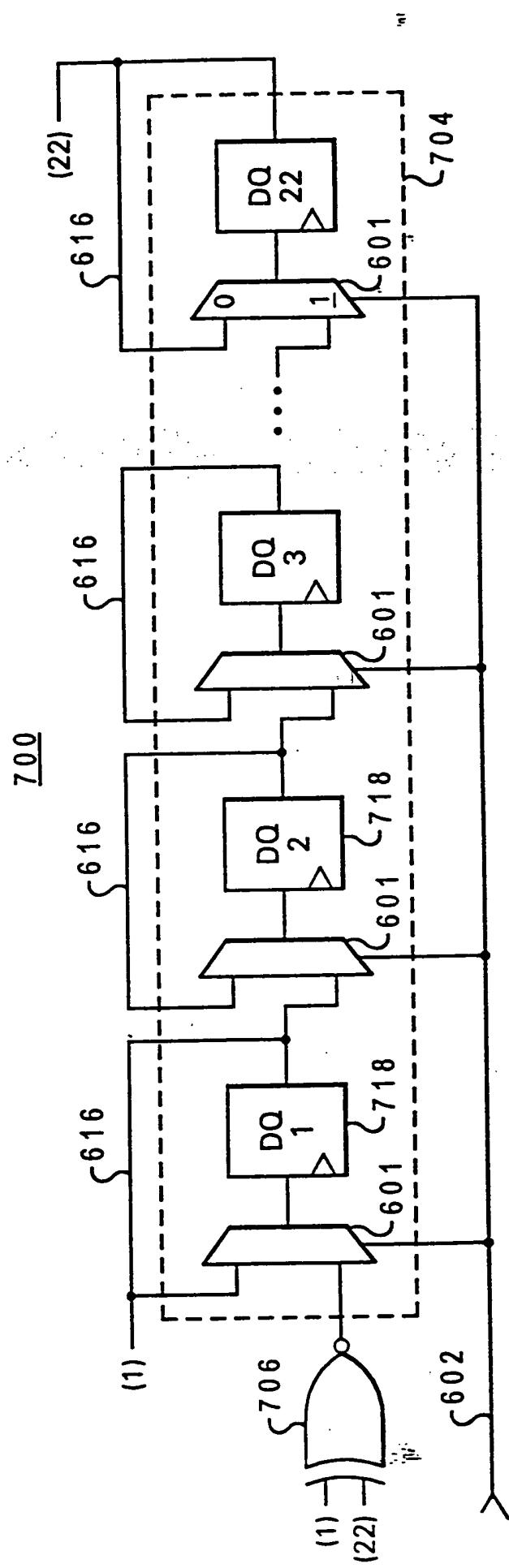


Fig. 7

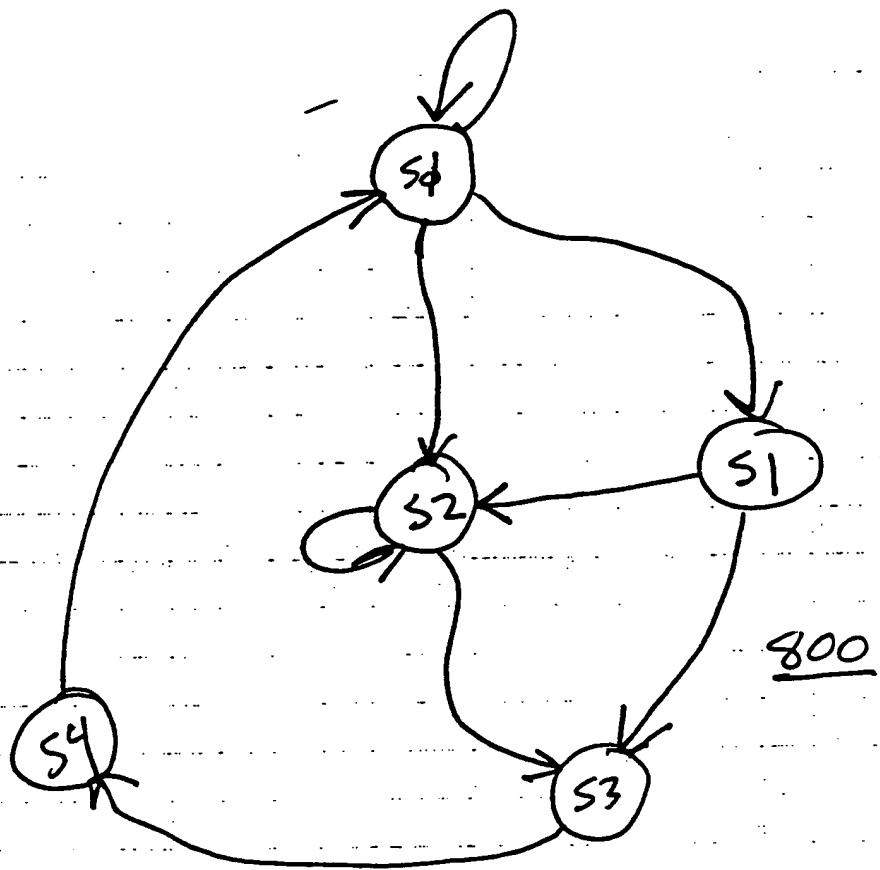


FIG. 8

(Prior Art)

entity fsm; fsm

850

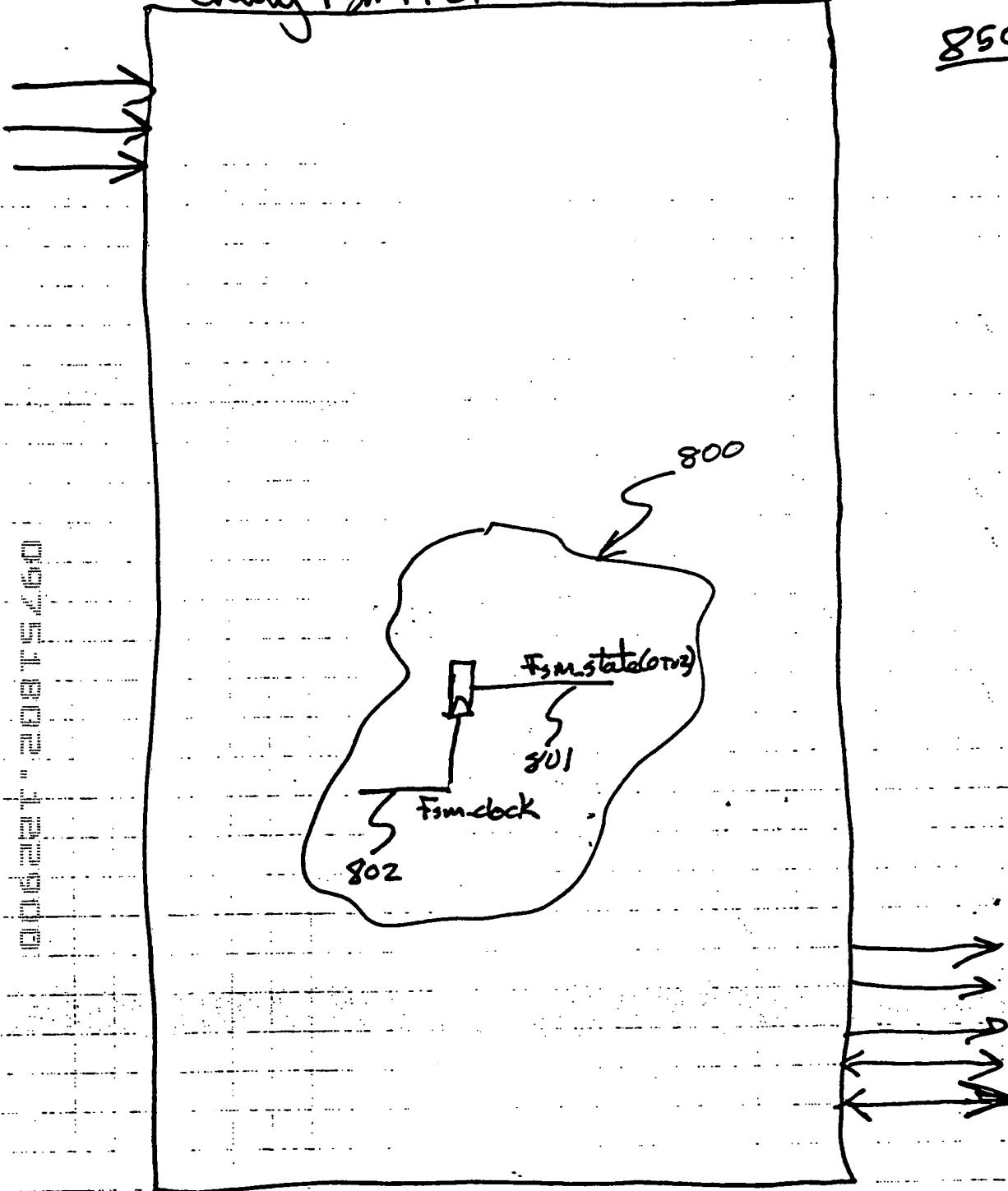


FIG. 8A  
(Prior Art)

entity fsm IS

PORT(

.... ports for entity fsm....

)j

ARCHITECTURE fsm of fsm IS

BEGIN

.... HDL code for fsm and rest of the entity...

fsm-state(0 to 2) <= ... signal 801...

853 {  
859 {  
854 {  
855 {  
856 {  
857 {

--!! Embedded fsm : examplefsm;  
--!! clock : (fsm\_clock);  
--!! static\_vector : (fsm-state(0 to 2));  
--!! states : (s0, s1, s2, s3, s4);  
--!! state\_encoding : ('000', '001', '010', '011', '100');  
--!! arcs : (s0 => s0, s0 => s1, s0 => s2,  
--!! arcs : s1 => s2, s1 => s3, s2 => s2,  
--!! arcs : s2 => s3, s3 => s4, s4 => s0);  
--!! end fsm;

} 852

86

END;

FIG. 8B

entity FSM:FSM

850

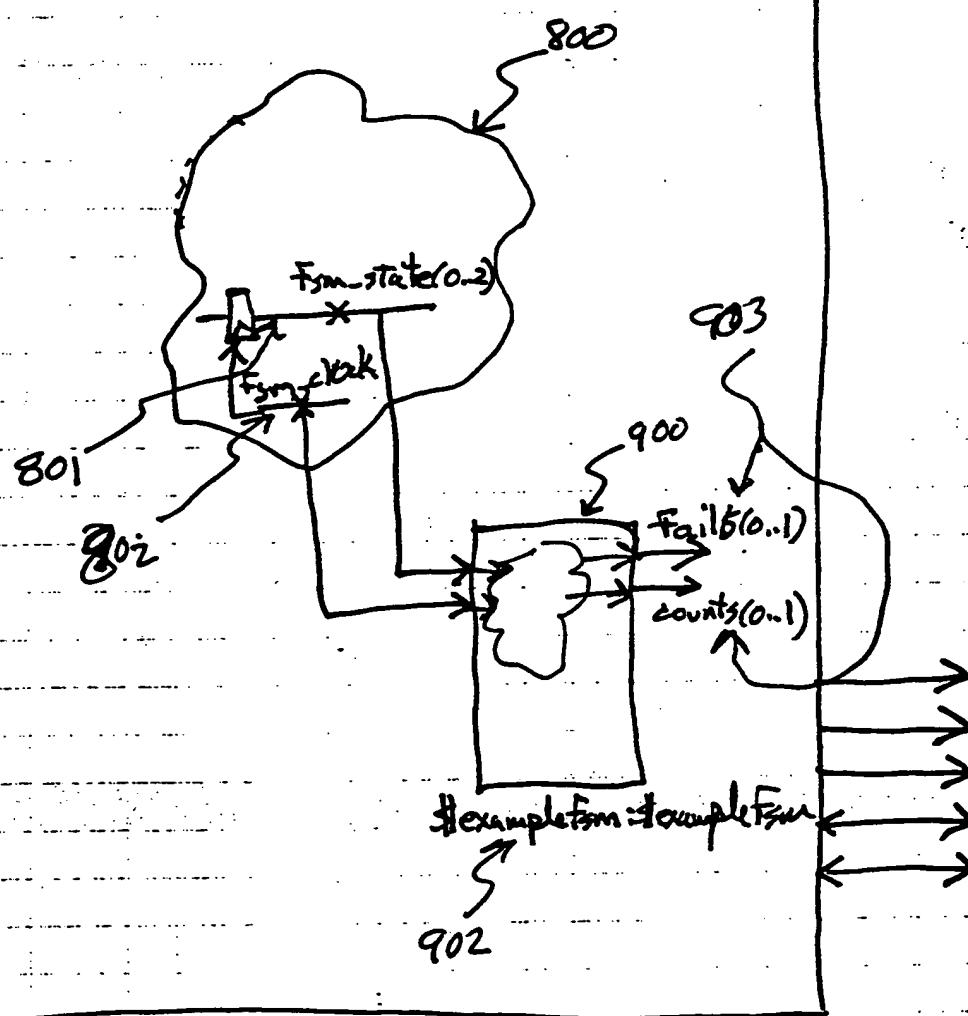


FIG. 9

TOP, TOP

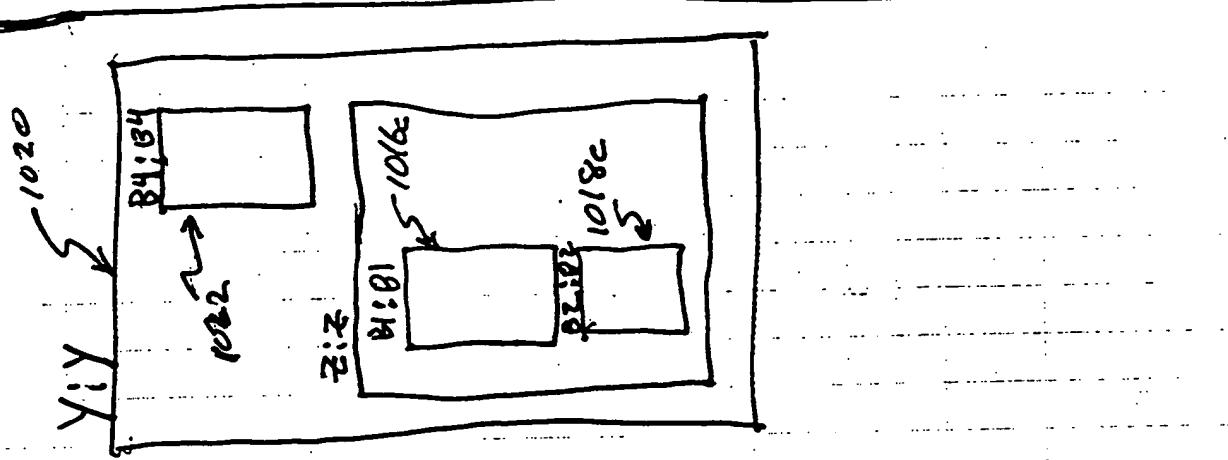
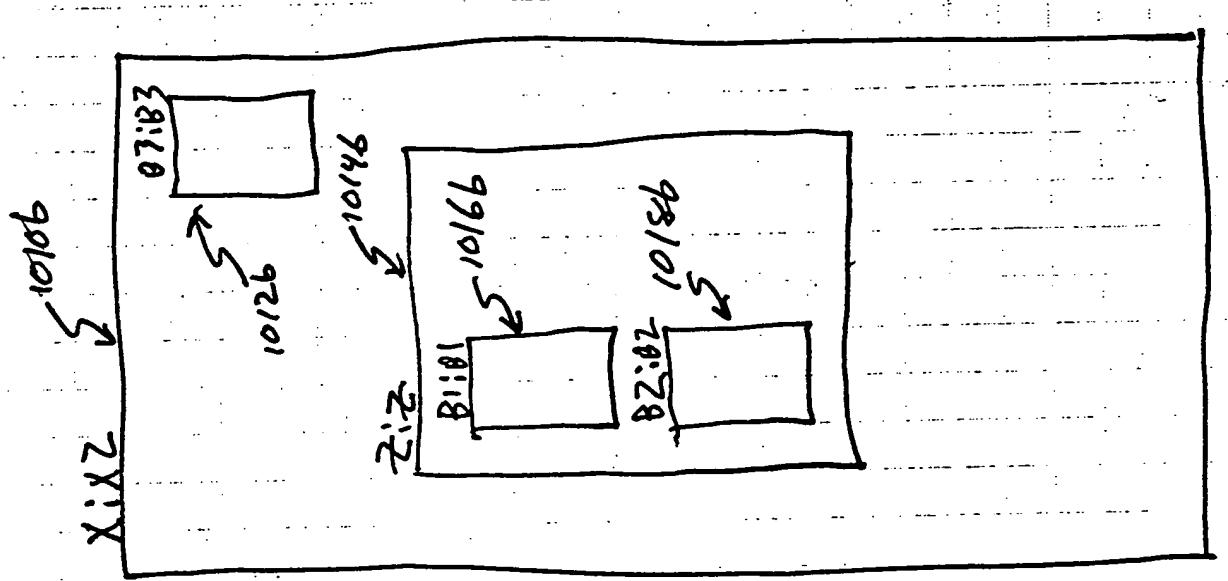
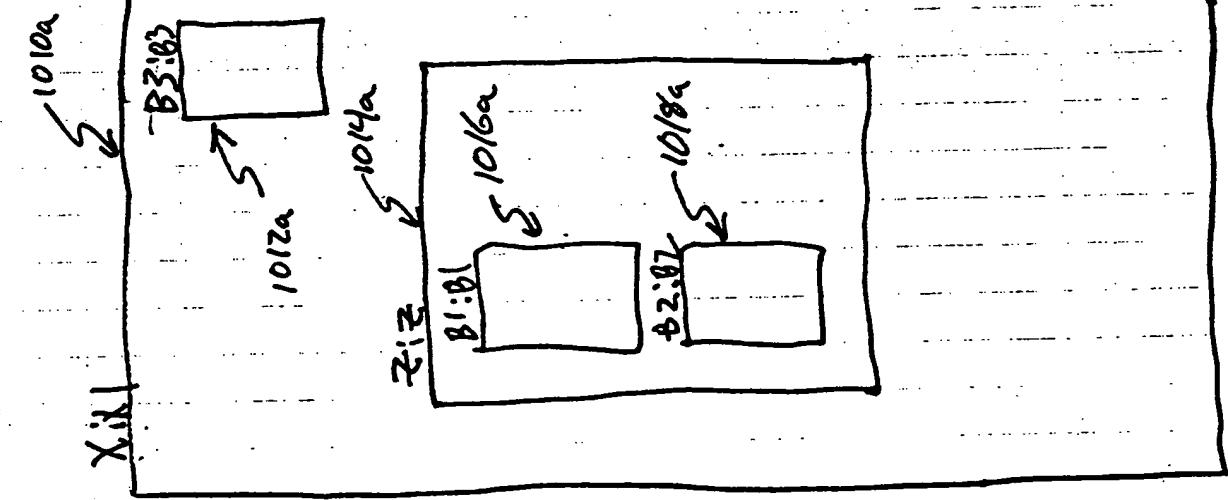


FIG. 10A

10303

instantiation identifier > . < instrumentation entity name > . < design entity name > . < event name >

10323

instantiation identifier > . < instrumentation entity name > . < design entity name > . < event name >

10343

instantiation identifier > . < instrumentation entity name > . < design entity name > . < event name >

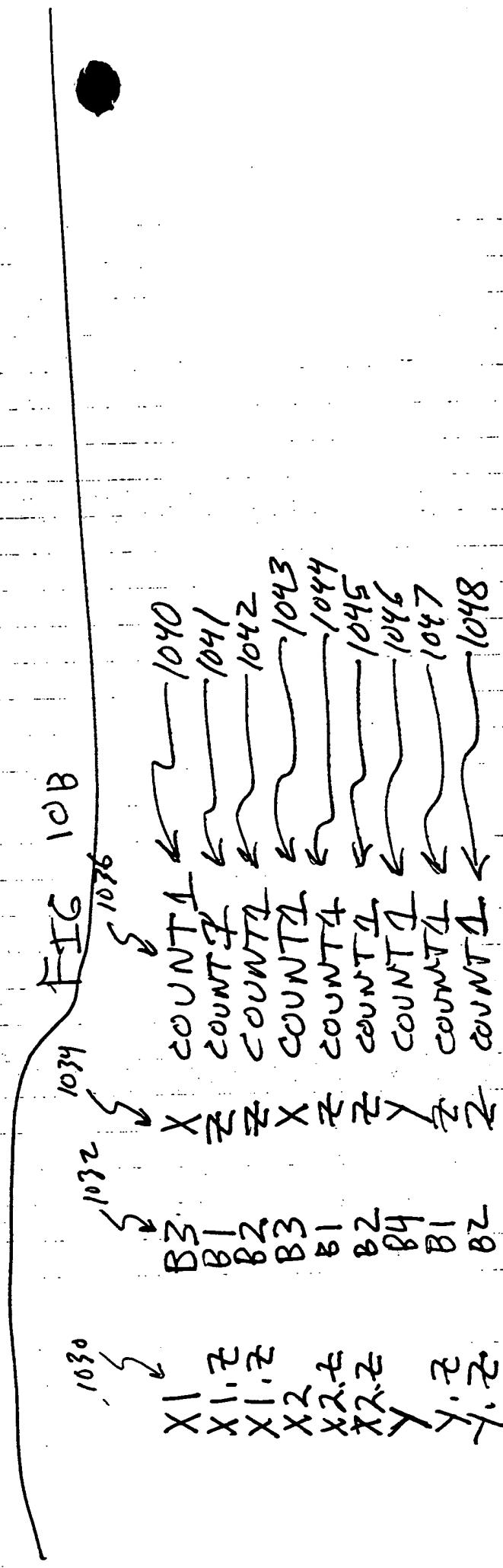


FIG 10C

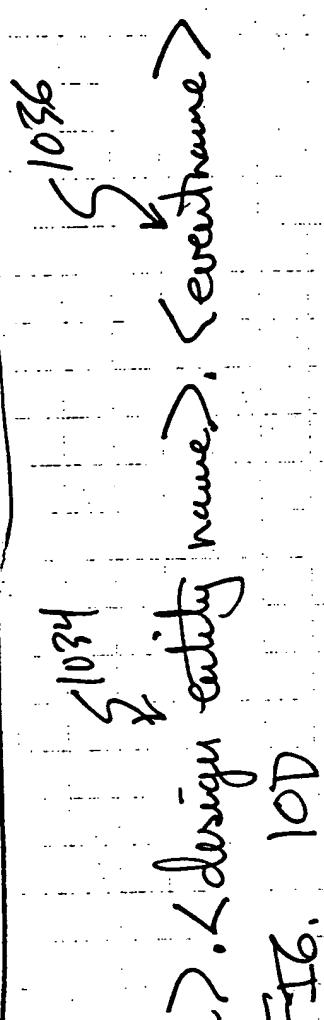


FIG 10D